

IN THE CLAIMS:

Claims 1-14 (canceled)

15. (Currently Amended) A bit pump having a transmit path and a receive path, comprising:
a precoder, coupled to said transmit path, to precondition ~~that preconditions~~ a transmit signal propagating along said transmit path;

a modulator, coupled to said precoder, to reduce ~~that reduces~~ a noise associated with said transmit signal;

an analog-to-digital converter, coupled to said receive path, to convert ~~that converts~~ a receive signal received at said bit pump into a digital format;

a decimator, coupled to said analog-to-digital converter, to downsample ~~that downsamples~~ said receive signal propagating along said receive path; and

an echo canceling system, coupled between said transmit and receive path, to attenuate ~~that attenuates~~ an echo in said receive signal, including:

a slave echo canceling stage to employ ~~that employs~~ a filter coefficient to attenuate said echo,

a separation circuit, coupled to said slave echo canceling stage, to generate ~~that generates~~ data representing a residual echo substantially exclusive of said receive signal, and

a master echo canceling stage, coupled to said separation circuit, to receive ~~that receives~~ said data and modify ~~modifies~~ said filter coefficient based thereon.

16. (original) The bit pump as recited in Claim 15 wherein said master and slave echo canceling stages receive said transmit signal, said transmit signal being delayed to said master echo canceling stage.

17. (Currently Amended) The bit pump as recited in Claim 15 wherein said separation circuit comprises an equalizer/slicer stage to determine ~~that determines~~ a symbol associated with said receive signal.

18. (Currently Amended) The bit pump as recited in Claim 17 wherein said separation circuit further comprises an estimator stage, coupled to said equalizer/slicer stage, to employ ~~that employs~~ said symbol and develop ~~develops~~ an estimated receive signal.

19. (original) The bit pump as recited in Claim 18 wherein master echo canceling stage generates an echo canceling signal and said separation circuit generates said data representing said residual echo as a function of said estimated receive signal, said echo canceling signal and a delayed receive signal.

20. (original) The bit pump as recited in Claim 15 wherein said master and slave echo canceling stages each comprise finite impulse response filters and infinite impulse response filters.

21. (original) The bit pump as recited in Claim 15 wherein said master and slave echo canceling stages each comprise a DC canceller.

22. (Currently Amended) A transceiver, comprising:

a framer to format ~~that formats~~ signals within said transceiver;

a bit pump coupled to said framer and having a transmit path and a receive path, including:

a precoder, coupled to said transmit path, to precondition ~~that preconditions~~ a transmit signal propagating along said transmit path;

a modulator, coupled to said precoder, to reduce ~~that reduces~~ a noise associated with said transmit signal;

an analog-to-digital converter, coupled to said receive path, to convert ~~that converts~~ a receive signal received at said bit pump into a digital format;

a decimator, coupled to said analog-to-digital converter, to downsample ~~that downsamples~~ said receive signal propagating along said receive path; and

an echo canceling system, coupled between said transmit and receive path, to attenuate ~~that attenuates~~ an echo in said receive signal, including:

a slave echo canceling stage to employ ~~that employs~~ a filter coefficient to attenuate said echo,

a separation circuit, coupled to said slave echo canceling stage, to generate ~~that generates~~ data representing a residual echo substantially exclusive of said receive signal, and

a master echo canceling stage, coupled to said separation circuit, to receive ~~that receives~~ said data and modify ~~modifies~~ said filter coefficient based thereon; and a controller to control ~~that controls~~ an operation of said framer and said bit pump.

23. (original) The transceiver as recited in Claim 22 wherein said master and slave echo canceling stages receive said transmit signal, said transmit signal being delayed to said master echo canceling stage.

24. (Currently Amended) The transceiver as recited in Claim 22 wherein said separation circuit comprises an equalizer/slicer stage to determine ~~that determines~~ a symbol associated with said receive signal.

25. (Currently Amended) The transceiver as recited in Claim 24 wherein said separation circuit further comprises an estimator stage, coupled to said equalizer/slicer stage, to employ that employs said symbol and develop ~~develops~~ an estimated receive signal.

26. (original) The transceiver as recited in Claim 25 wherein master echo canceling stage generates an echo canceling signal and said separation circuit generates said data representing said residual echo as a function of said estimated receive signal, said echo canceling signal and a delayed receive signal.

27. (original) The transceiver as recited in Claim 22 wherein said master and slave echo canceling stages each comprise finite impulse response filters and infinite impulse response filters.

28. (original) The transceiver as recited in Claim 22 wherein said master and slave echo canceling stages each comprise a DC canceller.